YAMAHA

DUAL CHANNEL POLYPHONIC SYNTHESIZER

CS70M

SERVICING GUIDE

CONTENTS

1. INTRODUCTION

The accompanying diagrams are block diagrams of the CS70M. The both block diagram covers the digital and analog stages.

Sections enclosed by [ ] in the digital block diagram denote individual functional units. A major feature of the CS70M is the 6-note polyphonic synthesizer with consonance performance capability. In addition, original tones can be generated with 39 different parameters in the front control panel, and stored in memory by "one-touch" operation of the 30 memory bank switches (in two series I and II). Furthermore, original tones can also be saved externally in special magnetic cards.

Other major features not found in more conventional synthesizers are enumerated below.

1. 6-note polyphonic system with "last-in-first-served" priority for notes. A 2-VCO per note chip is employed for source notes, and with series I and II, a total of 12 VCOs can be operated.
2. Notes generated by the 39 parameters in the control panel can be stored by write mode in the 30 memory banks (in series I and II), and then re-edited by the EDIT feature.
3. Melodies and consonance of up to 6 notes can be stored in 3.6Kbyte static RAMs at performing tempo. Memory capacity of the four memories A, B, C and D is approximately 600 notes.
4. Auto-tuning system for tuning by "one-touch" operation of 12 VCOs.

These functions are instructed by the CPU in accordance to a complex program, thereby ensuring speedy processing. Major CPU operations are outlined in Table 1 below.

These operations are processed sequentially by the program generated in assembler language in a 6Kbyte EP-EOM. The CS70M Keyboard Synthesizer with radically new features differes from conventional KAS system units in that the overall system is controlled by programmed CPU operation.

The main program flow chart is outlined on page 2. The CPU executes the program is accordance to this flow chart.

Major CPU Operations

1. KEYBOARD SWITCH ON/OFF SCANNING	2. AUTO TUNING
• Key code assignment • EXTERNAL key code control • Key code out • Portamento control • Glissando control • Hold control	3. NOR/SPLIT/UNISON MODE CHECK
	4. CARD READER CONTROL
	5. 39 CONTROL PARAMETERS READ/WRITE
	6. MEMORY BANK SWITCH SCANNING
	7. LED DRIVE CIRCUIT CONTROL
	8. SEQUENCER CONTROL
	9. EXTERNAL INPUT TERMINAL SCANNING

Table 1

Operational Flow Chart

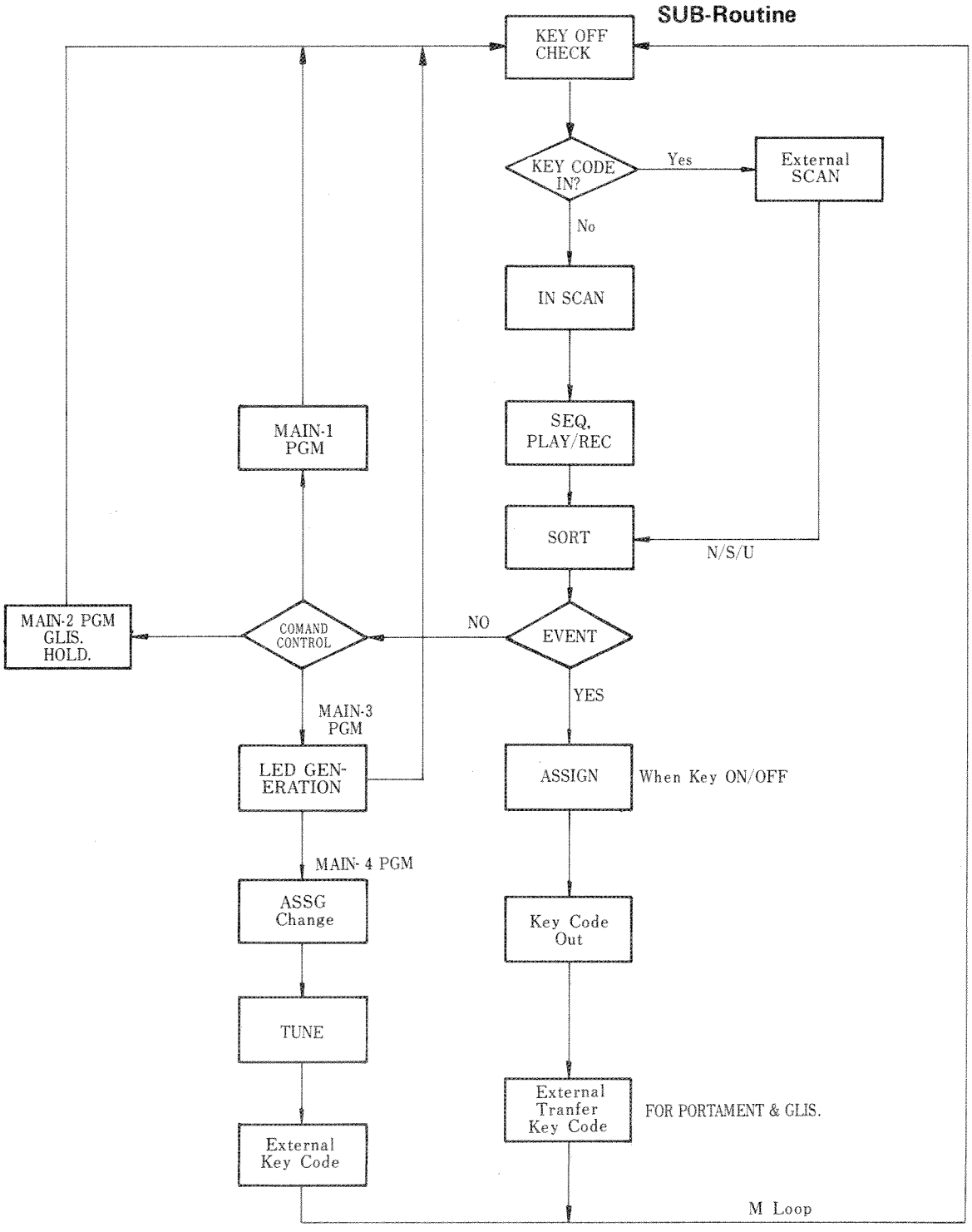


Fig. 1

MEMO

Brief Description of Overall Circuit Operation

The overall circuit composition is summarized in the OVERALL BLOCK DIAGRAM in Fig. 2. Firstly, an address signal is sent from the CPU to the address decoder via the address bus. 10 scanning bits for 10 and one half octave scanning are then generated in this decoder. Key switch on/off status in then checked by these 10 scanning bits, the scanning result by stored in the buffer amplifier, and the "key switch on/off data" being passed to the CPU via the CPU data bus.

On the basis of this data, the CPU subsequently addresses the key code data stored in the EP-ROM, the key code data being passed out via the data bus to a data selector where it is selected before being passed on to the D/A converters. The D/A converters include two types of MPX and DAC converters. One type is a keyboard voltage/note voltage converter equipped with an MPX stage, while the other type is a bias converter used to determine the bias for the auto tune circuit VCO and the control panel parameters. The keyboard operation voltage is generated in the first of the MPX stages (IC31), while the 12-note note voltages are generated in the next two MPX stages (IC32 and IC33). Similarly, the parameter and auto tune bias voltages are generated by converting the data selected by the data selector circuit, i.e. an 8-bit binary digital signal, into a DC current when passed through the DAC converter.

The respective analog signals obtained in this way appear as series I and series II VCO keyboard voltage outputs from the IC37 distributor. The outputs from the IC7, IC8, IC9 and IC10 distributors are the 39 tone parameter control voltages and the auto tuning mode VCO bias voltages, these output voltages being held by the S/H circuit for sampling purposes. The sample hold voltages are subsequently applied to the VCO, VCF and VCA circuits in much the same way as in conventional synthesizer circuits.

All of these operations are executed by the CPU main program. In card reader operation, however, the CPU checks the card reader every 1.6msec, and if a card reader interrupt instruction is detected, that instruction is executed immediately for card reader operation.

The Z80 memory address map is provided below for reference purposes. Note, however, that since A14 and A15 are not decoded in this model, address 4000 – FFFF involve repetition of addresses 0000 – 3FFF.

Memory Address Map

Addrss No.	ROM/RAM
0000–07FF	ROM IC 49
0800–0FFF	ROM IC 50
1000–17FF	ROM IC 51
1800–2BFF	Free
2000–2FFF (Timbre memory)	RAM IC 68,69
3000–33FF (SEQUENCER)	RAM IC 66,67
3400–37FF (SEQUENCER)(I/O)	RAM IC 70,71
3800–3BFF (SEQUENCER)	RAM IC 64,65
3000–3FFF (SEQUENCER)	RAM IC 62,63

Table 2

* Memory address map

In certain cases, address 0 – address 65536 (0000 – FFFF) will be stored in memory. The operation procedure program, for example, will be stored in 0000 – 17FF.

MK Matrix Table

	KBD0	KBD1	KBD2	KBD3	KBD4	KBD5	KBD6	KBD7	KBD8	KBD9
N 1	C_1	G_1	$C_2^\#$	G_2	$C_3^\#$	G_3	$C_4^\#$	G_4	$C_5^\#$	G_5
N 2	$C_1^\#$	$G_1^\#$	D_2	$G_2^\#$	D_3	$G_3^\#$	D_4	$G_4^\#$	D_5	$G_5^\#$
N 3	D_1	A_1	$D_2^\#$	A_2	$D_3^\#$	A_3	$D_4^\#$	A_4	$D_5^\#$	A_5
N 4	$D_1^\#$	$A_1^\#$	E_2	$A_2^\#$	E_3	$A_3^\#$	E_4	$A_4^\#$	E_5	$A_5^\#$
N 5	E_1	$B_1(H_1)$	F_2	$B_2(H_2)$	F_3	$B_3(H_3)$	F_4	$B_4(H_4)$	F_5	$B_5(H_5)$
N 6	F_1	C_2	$F_2^\#$	C_3	$F_3^\#$	C_3	$F_4^\#$	C_5	$F_5^\#$	C_6
N 7	$F_1^\#$									

Table 4

Memory Bank Circuit (Service Manual pp. 14 ~ 16, 32 ~ 34, 76, 77)

The control panel includes two sets of tone memory bank buttons (series I and series II) used for calling previously stored tones.
The 16th MANUAL button is used to switch the control panel to "set enable" status. Furthermore, tones generated by this MANUAL operation can be stored in the tone memory bank. When the panel WRITE button is switched on, the tones are stored in 2000 ~ 2FFF of the IC68/IC69 RAM IC memory address map.

Tones stored in this RAM can be reproduced ("called") by switching memory buttons 1 ~ 15 on. Furthermore, when calling these tones from memory, pressing any of the tone buttons a second time will activate the editing operation (in which case the corresponding LED lamp will start flashing on and off). During edit mode whereby the original tone is edited, the original tone stored in memory remains unchanged. This edit mode can be cancelled by pressing any desired memory bank switch. In addition, during this edit mode, edited tones can be stored in memory bank by WRITE mode operation.

Edit mode is not activated when MANUAL or EDIT is on for series I or series II.
Any original tone can be replaced by another desired tone by pressing the WRITE button during call mode (the new tone, however, must be in the same series).
The block diagram for the memory bank and peripheral circuits is outlined in Fig. 5.

When control panel memory bank SW1 is pressed, the panel switch address data is latched by IC58 via the data bus, and decoded by IC2. This decoded switch scanning bit is applied to the panel switch data input IC47 via the SW1 diode, resulting in the address input port no. 10 switch data being passed to the CPU, and the data for driving the LED corresponding to the memory switch is passed to IC56 LED cathode drive output port address no. 60 and the output port address no. 50 anode drive circuit. Consequently, the respective output voltages are passed via the data bus from the CPU, the latched positive voltage being applied to the LED cathode, and the negative voltage to the anode drive circuit. The respective drive transistors are thereby turned on, and the LED will light up.

The LED circuit is a matrix circuit, LEDs being turned on by LED driver combinations with the LED cathode and anode terminals. This matrix circuit is outlined in Table 5.
Tone data is stored in tone memory bank by the following operation. 4-bit data from the CPU is passed to output port IC58 address no.30 by each memory bank switch. The 4-bit data is latched by IC58 and decoded by the IC2 de-

coder. Then with 16-bit data decoded by this decoder, 30 memory bank switches, two MANUAL switches plus other switches are scanned. As a result, the data scanned by this operation is passed to the CPU, and the RAM addressed on the basis of that data. In the case of tone data, data stored between nos.20000 and 2FFF in the RAM address map is addressed, passed to the CPU, and then sent on to the next data selector circuit.

LED Matrix Circuit (Service Manual pp. 14 ~ 16)
LED matrix circuit low level denotes a voltage value from 0 to 0.5V. High level voltages are in the 2.5V to 5V range.
The LED matrix circuit consists of an 8-row by 8-column matrix. When signals (see waveforms in Fig. 6) are applied to CM0 ~ CM7, each LED in a column of 8 LEDs is selected separately on a time-sharing basis. And if the LE0 terminal is switched to high level when, say, the CM2 terminal in the 8 x 8 LED matrix table shown in Table 5 is at low level, the indicated LED will light up. The I/O address map for control panel LEDs is shown in the following chart.

I/O Address Map

Address	in / out	PORT
5 0	out	LED anode driver (IC57)
6 0	out	LED cathode driver (IC56)

The contents of bits 0 ~ 2 of the data written in address no.50 of IC57 are decoded by IC60, and obtained in negative logic at CM0 ~ CM7. The data written in address no.60 of IC56, on the other hand, is obtained at LE0 ~ LE7.

MAIN BANK AND LED BLOCK DIAGRAM

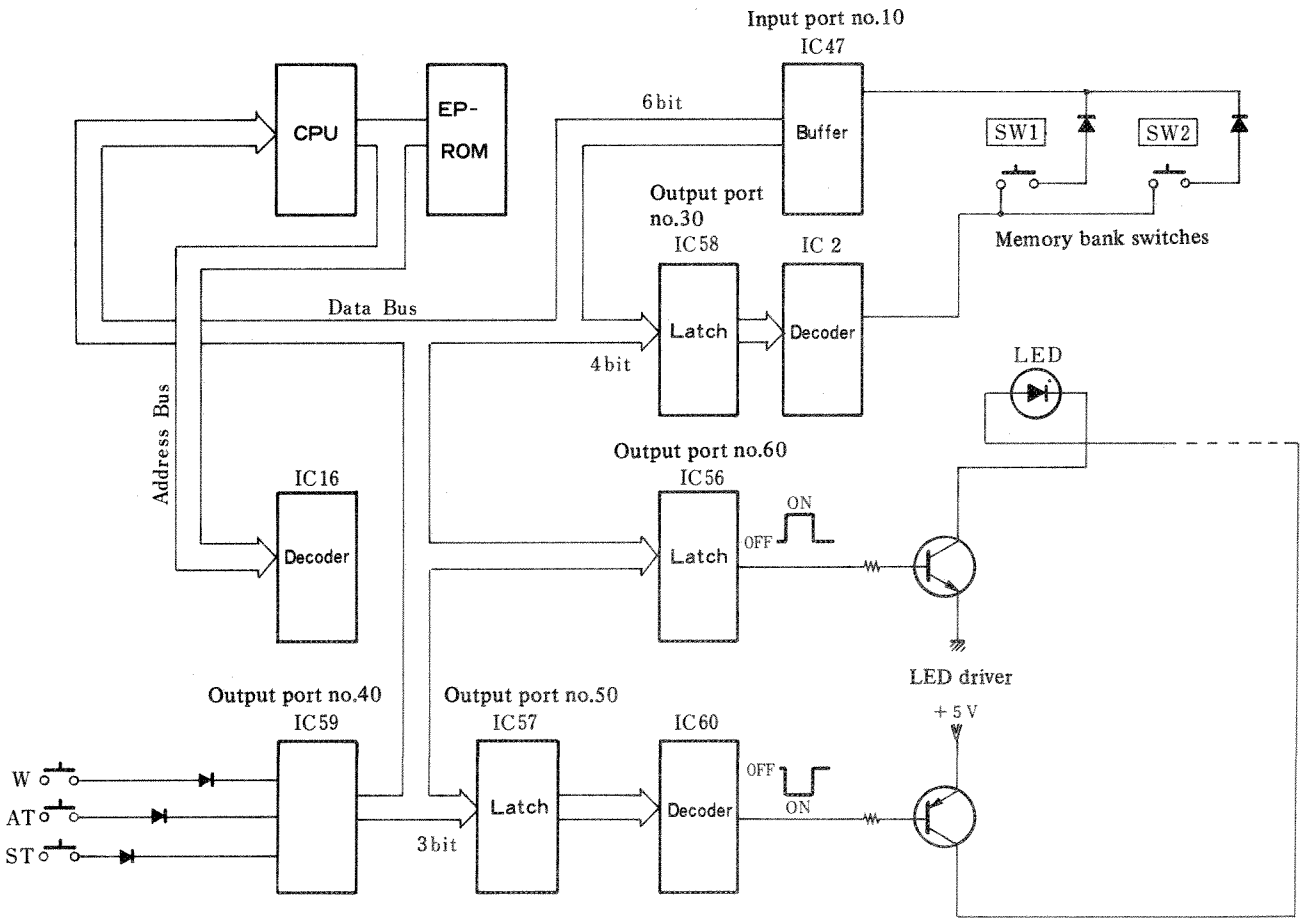


Fig. 5

CM0 ~ CM7 Terminal Voltage Waveforms

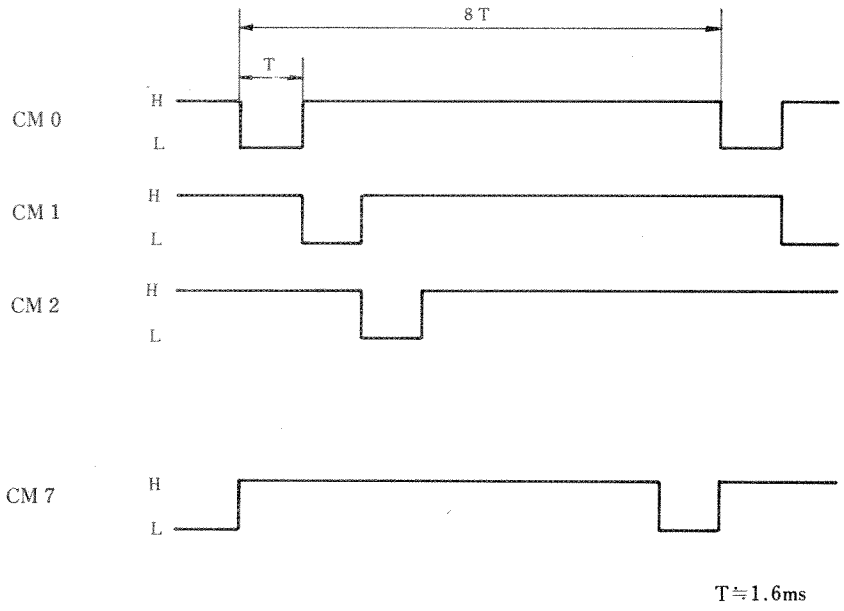


Fig. 6

8-Row x 8-Column Matrix Table

Terminal Name	LE 7	LE 6	LE 5	LE 4	LE 3	LE 2	LE 1	LE 0
CM0	I — 8 PSW75	I — 7 PSW74	I — 6 PSW73	I — 5 PSW72	I — 4 PSW71	I — 3 PSW70	I — 2 PSW69	I — 1 PSW68
CM 1	I — MANUAL PSW83	I —15 PSW82	I —14 PSW81	I —13 PSW80	I —12 PSW79	I —11 PSW78	I —10 PSW77	I — 9 PSW76
CM 2	II — 8 PSW91	II — 7 PSW90	II — 6 PSW89	II — 5 PSW88	II — 4 PSW87	II — 3 PSW86	II — 2 PSW85	II — 1 PSW84
CM 3	II — MANUAL PSW99	II —15 PSW98	II —14 PSW97	II —13 PSW96	II —12 PSW95	II —11 PSW94	II —10 PSW93	II — 9 PSW92
CM 4	TL 2	TL 3	TL 4	TL 5	TL 6	TL 7	TL 8	TL 9
CM 5	TL 1	TIME×5 PSW 50	I + II PSW 22	WHEEL PSW 23	VCO PSW 18	PW PSW 19	VCF PSW 20	VCA PSW 21
CM 6	◺ PSW35	⊓ PSW36	RMO PSW15	∿ PSW12	◺ PSW13	S/H PSW16	GLIDE+ PSW14	GLIDE− PSW17
CM 7	HP PSW39	BP PSW41	TIME×5 PSW40	⌣ PSW42	HOLD PSW51	WRITE PSW100	AUTO TUNE PSW101	STORE PSW102

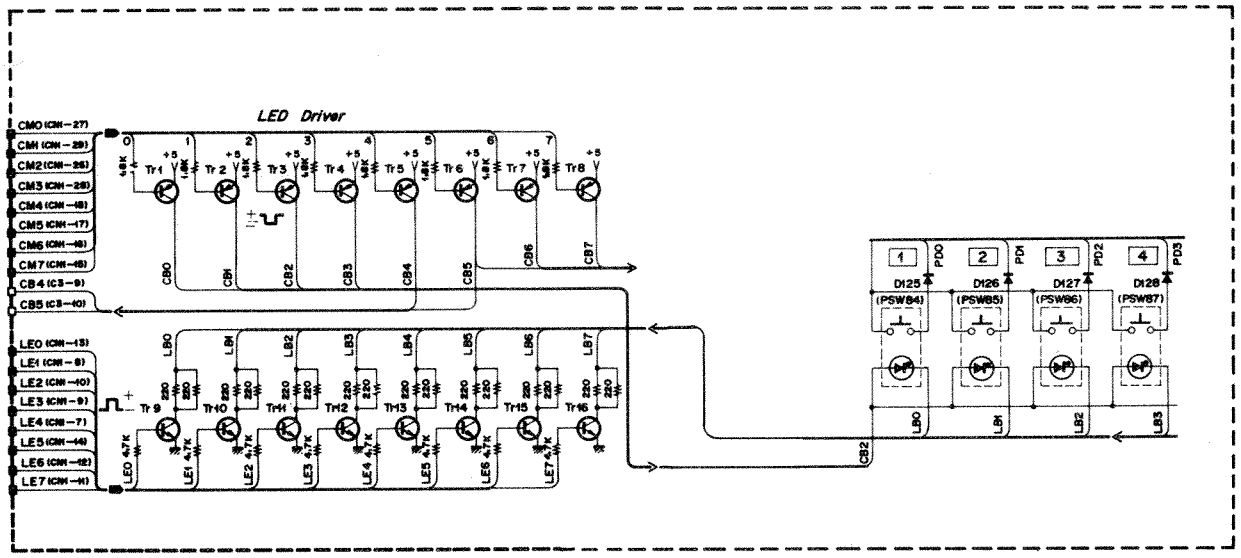
Lighted LED

Table 5

LED Drive Circuit (Service Manual pp. 14 ~ 16)
When PSW84 in Table 5 is switched on, a negative voltage appears at the CM2 terminal, and a positive voltage at the LE0 terminal according to the timing indicated in the following time chart. When these voltages are then applied to the respective LED driver transistors, +5V is applied to the LED, resulting in a flow of current and subsequent lighting up of the LED.

As can be seen from the circuit diagram, this LED drive circuit is a matrix circuit, and when +5V is applied to the CB2 and LB0 terminals, for example, the PSW84 LED is lit up.
With this LED 8 x 8 matrix circuit, any of the 64 LED lamps in the control panel can be switched on.

Panel Switch and LED Driver Circuit



Time Chart (for the PSW84 LED)

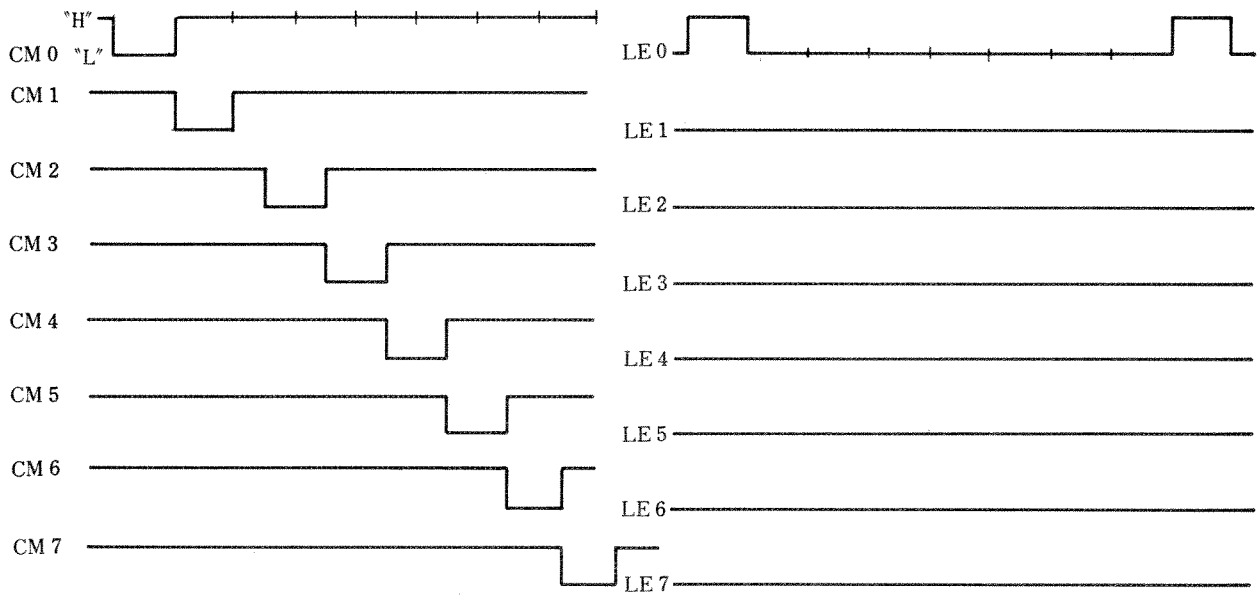


Fig. 6

Switching Matrix Circuit 1 (Service Manual pp. 14 ~ 16)

Low level voltages in this matrix circuit are in the 0 to 1V range. High level voltages are in the 4 to 5V range.
The bit 0 ~ bit 3 contents of the data written in I/O port address no.30 is obtained at the PAA ~ PAD terminals, while the bit 0 ~ bit 2 contents of the data written in I/O port address no.40 is obtained at the IS1 ~ IS3 terminals. And when I/O port address no.10 is read, the PD0 ~ PD5 terminal status is obtained in bit 0 ~ bit 5.

Panel Switch I/O Address Map

Address	in/out	PORT
3 0	out	Panel switch address (IC58)
4 0	out	Panel switch strobe (IC59)
1 0	in	Panel switch data (IC47)

Switching Matrix 1

IS1	IS2	IS3	PAA	PAB	PAC	PAD	Linear Encoder
H	L	H	H	L	L	H	PSW 10 DECAY
			L	H	L	H	PSW 38 NOISE
			H	H	L	H	PSW 37 PW
			L	L	H	H	PSW 11 MOD DEPTH
			H	L	H	H	PSW 7 SPEED
			L	H	H	H	PSW 9 ATTACK
			H	H	H	H	PSW 8 EG DEPTH
	H	L	H	L	L	L	PSW 57 VOLUME
			H	H	L	L	PSW 56 RELEASE
			L	L	H	L	PSW 55 SUSTAIN
			H	L	H	L	PSW 54 DECAY
			L	H	H	L	PSW 53 ATTACK
			H	H	H	L	PSW 52
			L	L	L	H	PSW 48 SUSTAIN
			H	L	L	H	PSW 47 DECAY
			H	H	L	H	PSW 49 RELEASE
			L	L	H	H	PSW 44 RESONANCE
			H	L	H	H	PSW 43 CUT OFF FREQ
			L	H	H	H	PSW 46 ATTACK
			H	H	H	H	PSW 45 EG DEPTH

Table 6

The relation between IS1 ~ IS3 and PAA ~ PAD is outlined in Table 6. When "H"/"L" combinations for these terminals are applied, the output voltages listed in Table 7 appear at PD0 ~ PD5 in accordance to the position of the linear encoder (also see Fig. 6). These voltages cannot be changed except by the linear encoder and panel switches.

Switch Matrix 1 Output Voltages

Top ↑ ↓ Bottom

PD5	PD4	PD3	PD2	PD1	PD0
L	H	H	H	H	L
L	L	H	H	H	L
L	L	L	H	H	L
L	H	L	H	H	L
L	H	L	L	H	L
L	L	L	L	H	L
L	L	H	L	H	L
L	H	H	L	H	L
L	H	H	L	L	L
L	L	H	L	L	L
L	L	L	L	L	L
L	H	L	L	L	L
L	H	L	H	L	L
L	L	L	H	L	L
L	L	H	H	L	L
L	H	H	H	L	L
L	H	H	H	L	H
L	L	H	H	L	H
L	L	L	H	L	H
L	H	L	H	L	H
L	H	L	L	L	H
L	L	L	L	L	H
L	L	H	L	L	H
L	H	H	L	L	H
L	H	H	L	H	H
L	L	H	L	H	H
L	L	L	L	H	H
L	H	L	L	H	H
L	H	L	H	H	H
L	L	L	H	H	H
L	L	H	H	H	H
L	H	H	H	H	H

H≒9.4V, L≒0V

The statuses listed in this table appear consecutively when the slide control is operated.

Table 7

Switching Matrix Circuit 2

When "H"/"L" voltage combinations as listed in Table 8 are applied to the IS1 ~ IS3 and PAA ~ PAD terminals, the terminal corresponding to one of the PD0 ~ PD5 switches will be switched to "H" level once the relevant "PSW" is switched on.

Switching Matrix Circuit 3

When "H"/"L" voltage combinations as listed in Table 9 are applied to the IS1 ~ IS3 and PAA ~ PAD terminals, the indicated terminal will be switched to "H" level.

Switching Matrix 3

IS1	IS2	IS3	PAA	PAB	PAC	PAD	"H" level terminal
L	H	H	L	L	L	X	FTX (C4—5)
			H	L	L	X	FTY (C4—6)
			L	H	L	X	AST (C4—7)
			H	H	L	X	POR (C4—2)
			H	L	H	X	SEQ (C4—1)
			L	H	H	X	BNK (C4—3)
			H	H	H	X	TMP (C4—4)

Note 1. "H" level possible in X positions

Table 9

Switching Matrix 2

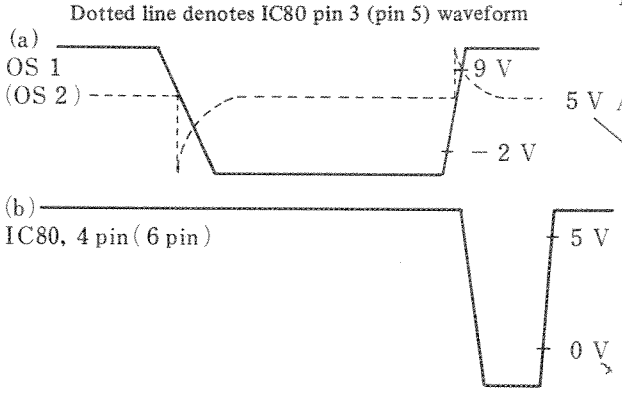
IS1	IS2	IS3	PAA	PAB	PAC	PAD	PD5	PD4	PD3	PD2	PD1	PD0
L	H	H	L	L	H	X			TS4	TS3	TS2	TS1
H	L	H	L	L	L	L			PSW 87 II—4	PSW 86 II—3	PSW 85 II—2	PSW 84 II—1
			H	L	L	L			PSW 75 I—8	PSW 74 I—7	PSW 73 I—6	PSW 72 I—5
			L	H	L	L			PSW 71 I—4	PSW 70 I—3	PSW 69 I—2	PSW 68 I—1
			H	H	L	L			PSW 91 II—8	PSW 90 II—7	PSW 89 II—6	PSW 88 II—5
			L	L	H	L			PSW 79 I—12	PSW 78 I—11	PSW 77 I—10	PSW 76 I—9
			H	L	H	L			PSW 83 I—MANUAL	PSW 82 I—15	PSW 81 I—14	PSW 80 I—13
			L	H	H	L			PSW 99 II—MANUAL	PSW 98 II—15	PSW 97 II—14	PSW 96 II—13
			H	H	H	L			PSW 95 II—95	PSW 94 II—94	PSW 93 II—93	PSW 92 II—92
			L	L	L	H	PSW 35 ⌐	PSW 36 ⌐¬	PSW 39 HP	PSW 41 BP	PSW 40 TIME×5	PSW 42 ⌐¬
H	H	L	L	L	L	L	PSW 15 RMO	PSW 12 ∿	PSW 13 ⌐	PSW 16 S/H	PSW 14 GLIDE+	PSW 17 GLIDE−
			L	H	L	L	PSW 18 VCO	PSW 19 RW	PSW 20 VCF	PSW 21 VCA	PSW 22 I+II	PSW 23 WHEEL
			L	H	L	H		PSW 50 TIME×5	PSW 51 HOL—D	PSW 100 WRITE	PSW 101 AUTO TUNE	PSW 102 STORE

Note 1. Both H and L are possible in the X positions.
Note 2. There are no corresponding switches for sections left blank.

Table 8

Data Latching Circuit/OS Input Differential Circuit (Service Manual pp. 38 ~ 41)

When pulse (a) is applied to OS1 or OS2, waveform (b) appears at pins 4 and 6 of IC80.



Address Decoder Circuit (Service Manual pp. 38 ~ 41)

When the above pulse signal is applied to OS1 or OS2, the DB0 ~ DB7 contents are written in the D-FF IC listed in the following table in accordance to the AO0 ~ AO3 combination. The writing timing is controlled by the CPU. Note, however, that DB0 ~ DB7 are the terminals which invert terminals DO0 ~ DO7 by the IC54 buffer.

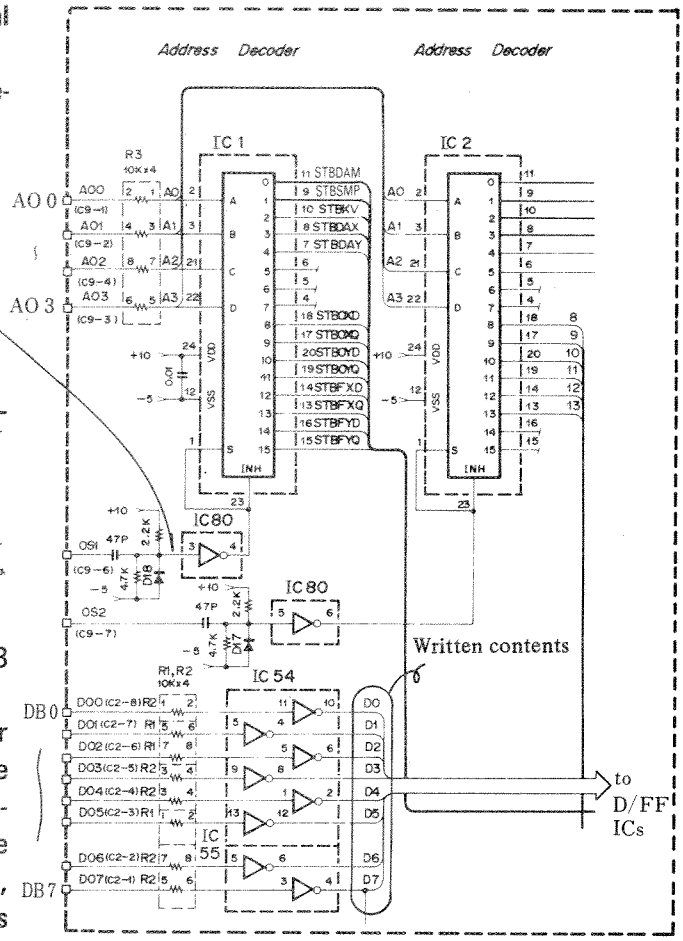


Fig. 7 Address Decoder Circuit

Table 10

AO 3	2	1	0	OS 1	OS 2
0	0	0	0	IC 5	1/2 IC53 (ATCN)
0	0	0	1	IC 6	1/2 IC53 (LTG)
0	0	1	0	IC 34, 35	IC 3
0	0	1	1	IC 12, 13	IC 4
0	1	0	0	IC 24, 25	1/2 IC52 (PRTD)
0	1	0	1	—	1/2 IC52 (PRTQ)
0	1	1	0	—	—
0	1	1	1	—	—
1	0	0	0	IC 17	1/2 IC50 (RST 1)
1	0	0	1	IC 15	1/2 IC50 (RST 2)
1	0	1	0	IC 29	1/2 IC51 (RST 3)
1	0	1	1	IC 27	1/2 IC51 (RST 4)
1	1	0	0	IC 18	1/2 IC49 (RST 5)
1	1	0	1	IC 16	1/2 IC49 (RST 6)
1	1	1	0	IC 30	—
1	1	1	1	IC 28	—

Level Shift Circuit (Service Manual pp. 32 ~ 34)

The following waveform is obtained when data is written in I/O address 00 ~ 1F. The address, IORQ and WR timing conforms with the Z80 specifications.

The waveform shown in the following diagram appears at OS1 when the address is from 00 to 0F, and at OS2 when address is from 10 to 1F. The side not selected is kept at +10V. This output waveform appears at the level shifter outputs AO0 ~ AO3 and DO0 ~ DO7 when the corresponding NAND and NOR outputs are at "1" level. For "0" level, however, the output terminals are kept at –5V.

The level shift buffer amplifier is a 2-stage transistor circuit (see Fig. 8).

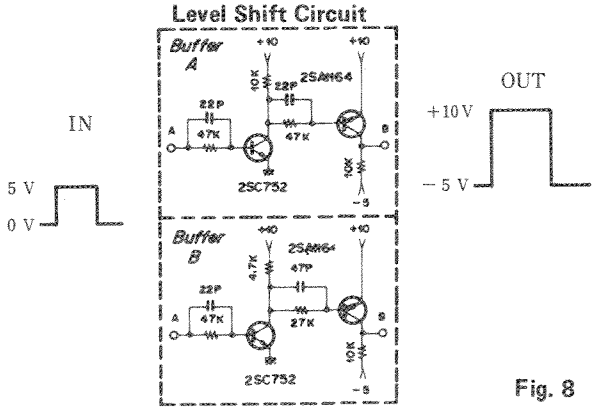
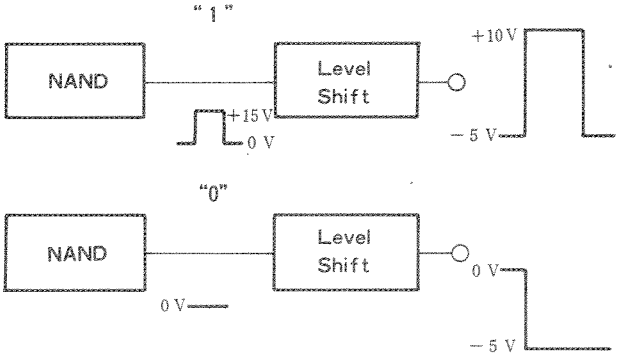
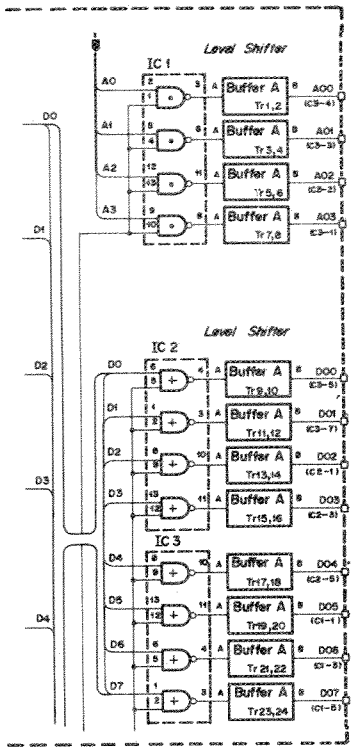


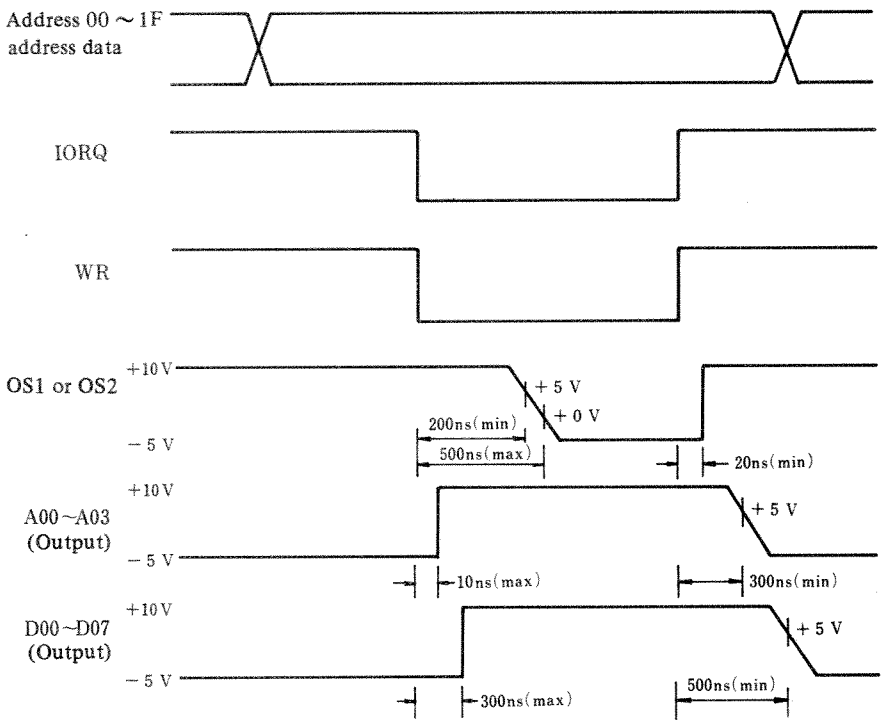
Fig. 8

Buffer amplifier input A is connected to a NAND, a "1" output resulting in a positive voltage being applied to A. Transistor 2SC752 is thereby forward biased (i.e. turned on), followed by 2SA1164 also being turned on. The output is thereby changed from –5V to +10V. Since the operating voltage for the CPU board is obtained from a 5V power supply, level shifting is required for circuit connections with other circuit boards.





Level Shift Circuit



Address, IORQ and WR Time Chart

D/A Converter Circuit (Service Manual pp. 38 ~ 41) (Tone and VCO bias DAC)

Data is written in IC12 and IC13 (IC24 and IC25) by the method described in the address decoder description. When this data is expressed as a numerical value n with DB0 as the LSB and DB7 as the MSB, a voltage Vx (Vy) determined by the following formula is obtained at pin 1 of IC59 (pin 14 of IC45). n is varied stepwise from 0 up to 255.

$Vx[Vy] = n/25.6 \pm 0.05V \pm 2\%$

where Vx is the series I voltage, and

Vy the series II voltage.

$(0 \leqq n \leqq 255)$

When n is increased in single steps, Vx(Vy) is also increased in single steps.

The ICs used in the D/A converters are single-chip ICs designed to convert 8-bit binary encoded digital signals into analog DC currents. An actual circuit is outlined in Fig. 9.

The output voltage from pin 1 of IC59 (pin 14 of IC75) is passed to the de-multiplex stage of the next circuit where an 8-channel analog switching circuit is controlled by D0 ~ D2 digital signals from IC5, and divided into tone analog voltages and M board VCO bias voltages etc. This stage is known as the distributor (see circuit diagram in Fig. 12).

D/A Converter Circuit (MPX) (For Key Volt)

Data is written in IC34 and IC35 in accordance to Table 10 as described in the address decoder description. This data is expressed as a numerical value m (hexadecimal notation) with DB0 as the LSB and DB7 as the MSB. In the case of a key volt voltage, the 8-channel analog switching circuit is controlled by three IC34 digital signals in order to obtain an octave signal. In this case, however, the 4 LSB bits of m (LSBD0 ~ D3) and the MSB (MSBD7) are not involved in Table 11.

For example, when m = 20, VR1 is adjusted so as to obtain a voltage of 125.0 ± 0.1mV on pin 6 of IC38. And when the values of m are changed, the voltages listed in Table 11 are obtained.

Key Volt Voltages [mV]

m	00	10	20	30	40	50	60	70
I C38 (6pin)	62.5 mV	62.5 mV	125 mV	250 mV	500 mV	1000 mV	2000 mV	4000 mV

Table 11

DAC Circuit

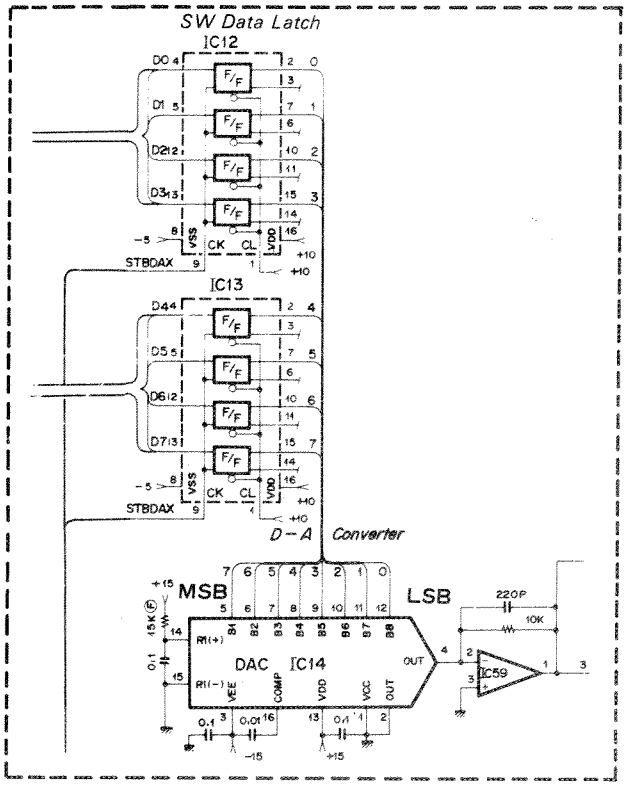


Fig. 9

Key Volt D/A Converter Circuit

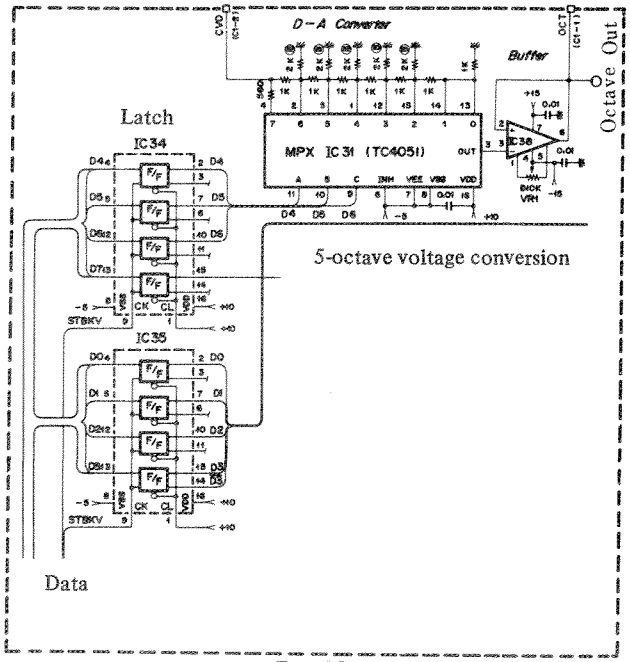


Fig. 10

Note Voltage Circuit (Service Manual pp. 38 ~ 41)

With m = 2E, VR2 is adjusted to obtain a voltage of 125mV on pin 6 of IC39. And when m is changed, the voltage obtained from bits 4 ~ 6 of m, plus the multiplication product obtained from bits 0 ~ 3 (i.e. the voltage obtained by D4 ~ D6 – see Table 11, and the multiplication product Vk obtained from D0 ~ D3 ($\overline{D3}$) are obtained at pin 6 of IC39.

Note Voltage

4 LSB in m	0	1	2, 3	4	5	6, 7
Multiplication factor	0.5297	0.5612	0.5946	0.6300	0.6674	0.7071
Note	C#	D	D#	E	F	F#
4 LSB in m	8	9	A, B	C	D	E, F
Multiplication factor	0.7492	0.7937	0.8409	0.8909	0.9439	1.0000
Note	G	G#	A	A#	B	C

Table 12

For example, when there is an output voltage of 4000mV at pin 6 of IC38 (see Table 11), the C# voltage will be 4 x 0.5297V = 2.119V, while the C voltage will be 4V (since the multiplication factor is 1). These voltages are passed to the VCO as note voltages.

The IC32/IC33 MPX contains bit 3 and the chip-inhibit control bit D3 or $\overline{D3}$. A 12-note note voltage for a single octave is generated by these two ICs, each IC generating note voltages for 6 notes. For 6 or more notes, an INH bit is applied to D3 or $\overline{D3}$ in order to select the IC chip.

Note Voltage D/A Converter Circuit

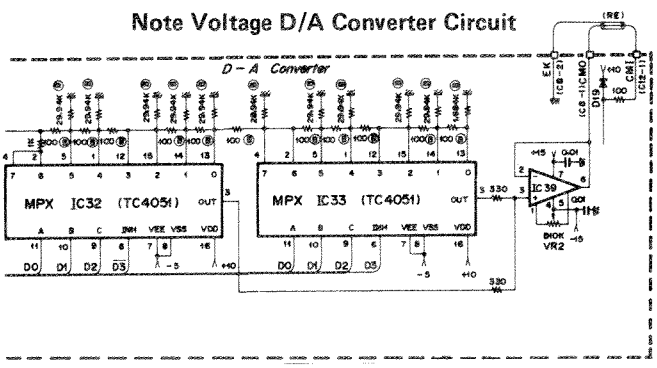


Fig. 11

Series I [II] Sample Hold Circuit (Service Manual pp. 38 ~ 41)

The note data voltage S/H circuit performs the sample/hold operation according the following procedure.

STEP 1 i = 0 is set (program parameter number).

STEP 2 Data ni is written in IC12 and IC13 [IC24 and IC25] (Denotes which number parameter data)

STEP 3 Write Table 13 (Table 14) ai into IC5. (D0, D1, D2)

STEP 4 Write Table 13 (Table 14) si into IC6 after a delay of 1.5μsec. (SMPLD1 ~ SMPLTN)

STEP 5 Write all bits "1" data into IC6 after a delay of 1.6msec.

STEP 6 With i = i + 1, return to STEP 1 when i = 40, but return to STEP 2 when i = 40.

In other words, the Table 13 (Table 14) voltage can be obtained at any output for any desired combination of ni (where $0 \leqq i \leqq 39$).

Distributer and S/H Circuit

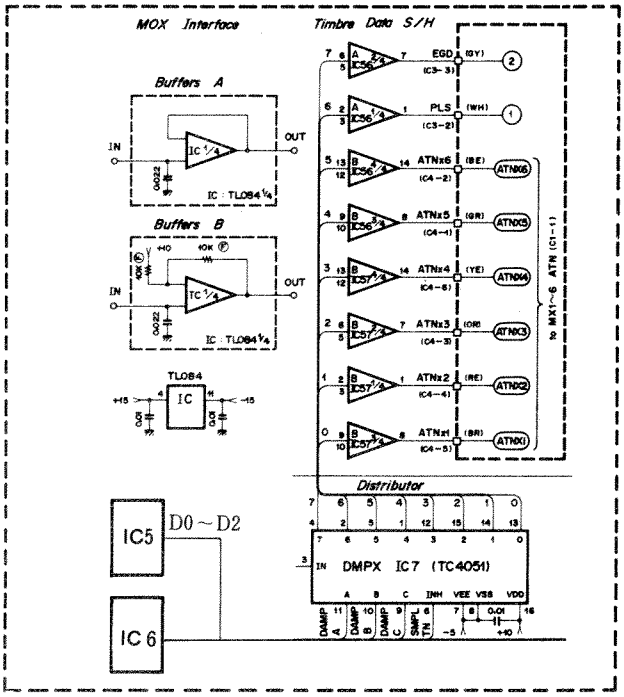


Fig. 12

Table 13

Parameter / IC12.13 / ni	IC6 D4~D0 si bit 43210	IC5 D2D1D0 ai bit210	Output Pin		Voltage
0	11110	000	IC 65	pin 8	Va
1		001	65	14	
2		010	65	7	
3		011	64	14	
4		100	62	14	
5		101	64	1	
6		110	63	1	
7		111	63	14	
8	11101	000	62	7	
9		001	65	1	
10		010	63	8	
11		011	63	7	
12		100	64	7	
13		101	62	8	
14		110	64	8	
15		111	—	—	
16	11011	000	61	8	
17		001	62	1	
18		010	61	7	
19		011	61	14	
20		100	59	14	
21		101	60	1	
22		110	60	8	
23		111	60	14	
24	10111	000	58	8	
25		001	60	7	
26		010	58	14	
27		011	59	7	
28		100	61	1	
29		101	58	7	
30		110	59	8	
31		111	58	1	
32	01111	000	57	8	Vb
33		001	57	1	
34		010	57	7	
35		011	57	14	
36		100	56	8	
37		101	56	14	
38		110	56	1	Va
39		111	56	7	Va

Va(n) = Vx(n) ± 0.05 VOLT
Vb(n) = 2Vx(n) − 10 ± 0.1 VOLT ± 2%
Vx: refer to section on D/A converter circuit (DAC).

Table 14

Parameter / IC24.25 / ni	IC6 D4~D0 si bit 43210	IC5 D2D1D0 ai bit210	Output Pin		Voltage
0	11110	000	IC 72	pin 8	Va
1		001	72	14	
2		010	75	8	
3		011	75	7	
4		100	70	1	
5		101	71	8	
6		110	70	14	
7		111	72	1	
8	11101	000	72	7	
9		001	75	1	
10		010	71	7	
11		011	70	8	
12		100	71	1	
13		101	70	7	
14		110	71	14	
15		111	—	—	
16	11011	000	66	1	
17		001	66	7	
18		010	69	14	
19		011	69	8	
20		100	67	1	
21		101	68	14	
22		110	68	8	
23		111	69	1	
24	10111	000	66	8	
25		001	68	7	
26		010	68	1	
27		011	67	8	
28		100	69	7	
29		101	66	14	
30		110	67	14	
31		111	67	7	Vc
32	01111	000	74	1	Vb
33		001	74	14	
34		010	74	7	
35		011	74	8	
36		100	73	14	
37		101	73	8	
38		110	73	1	Va
39		111	73	7	Va

Va(n) = Vy(n) − 10 ± 0.05 VOLT
Vb(n) = 2Vy(n) − 10 ± 0.1 VOLT ± 2
Vc(n) = Vy(n) ± 0.3 VOLT
Vy: refer to section on D/A converter circuit (DAC).

Key Volt S/H Circuit (Service Manual pp. 38 ~ 41)

The sample hold operation is performed by the following procedure after writing 0 into IC52 (PRTD, PRTQ) according to the data latch circuit.

STEP 1 i = 0

STEP 2 Write data m into IC34 and IC35. (Denotes which M board for what octave and what interval).

STEP 3 Write Table 15 ai into IC5.

STEP 4 Write Table 15 si into IC6 after a delay of 15μsec.

STEP 5 Write all bits "1" data into IC6 after a delay of 35μsec.

STEP 6 With i = i + 1, return to STEP 1 after a delay of 1.2msec when i = 7, but return to STEP 2 after a delay of 5μsec when i = 7.

Output Voltages and Adjustment Controls for mi Changes

	IC6 D4 ~ D0	IC5 D2D1D0		Adjustment Control
IC34, 35 / mi	si bit 543210	ai bit 210	Output Pin	VR
0	011111	000	CV1	VR3
1		001	CV2	VR4
2		010	CV3	VR5
3		011	CV4	VR6
4		100	CV5	VR7
5		101	CV6	VR8
6		110	CVS	VR9

Table 15

Key Volt Distributor and S/H Circuit

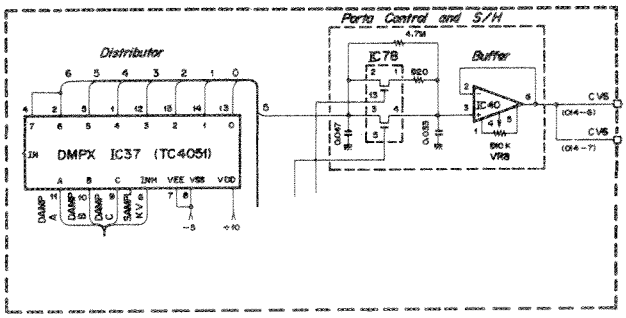


Fig. 13

Auto Tune Circuit (Service Manual pp. 20 ~ 22, 32 ~ 34, 46 ~ 49, 76, 77)

When the AUTO TUNE button is switched on, sound generation is inhibited for about 1 second while the 12 M boards are automatically tuned. If any of the tone memory bank switches (tone panel switches 1 to 6) lights up after this auto tuning operation, inability for the M board corresponding to that switch number to proceed with automatic tuning is indicated.

The automatic tuning range for M boards is ±30%. The AUTO TUNE block diagram is outlined in Fig. 14.

When the AUTO TUNE button in pressed, M board data for sound generation is passed via the data bus from the CPU, D/A converted in the MPX stage, and then applied to the M board. This data is 8', and the sound name is an A3 square wave. The frequency of the generated sound is applied to the ATSG pin (see block diagram) and latched by D-FF. The clock frequency for this latching circuit is 2.5MHz, output of input D being obtained by this clock. There are two D-FF latching circuits, these using the ϕ and $\overline{\phi}$ clocks.

These outputs, $\overline{Q1}$ and Q2 are subjected to a NAND operation by the count data latch pulse generator circuit, resulting in the generation of a pulse signal for latching of the count data. This NAND output is subsequently integrated by a CR circuit into the waveform shown in the time chart, this signal being applied to the next NAND circuit (IC5). Hence, the counter reset pulse is generated by this integrated waveform (see the time chart in Fig. 15).

Counters A and B count the master clock, the corresponding outputs being accepted by the latching circuit by the count data latch pulse generator circuit pulse signal generated on the basis of the reference frequency. That is, the least significant 11 bits of the value obtained by dividing the square wave cycle period (applied to ATSG) by TCK are written into IC12 and IC13 by the leading edge of the IC5 (pin 11) pulse.

The CPU reads this data by reading I/O addresses 18 and 19 via IC7, IC8 and IC9. The data ready flag (IC15 1/2) is set by the leading edge of the IC5 (pin 8) pulse, reset by the CPU I/O address 00 write instruction, and obtained in bit 5 of the I/O address 18 data select output. As a result, the D0 ~ D5 output is passed to the CPU via the data bus. In this way, the 12 M boards in series I and series II are checked sequentially. The counted results are rearranged in order from low numbers upwards in the CPU, and with the third lowest item of data as a reference, data for compensating differences from that reference is passed out via the data bus. This data is then D/A converted, and subsequently used in determining the VCO bias. And once this bias is decided, the corresponding data is stored by the CPU, and remains unchanged until the AUTO TUNE button is pressed again. When tuning M boards, care must be taken not to switch the AUTO TUNE button on.

I/O Address Map Involved in Auto Tuning

Address	in/out	PORT
0 0	out	Flag setting
1 8	in	Synchronization data (IC7, IC8, IC9)
1 9	in	Synchronization data (IC7, IC8, IC9)

● AUTO TUNE BLOCK DIAGRAM

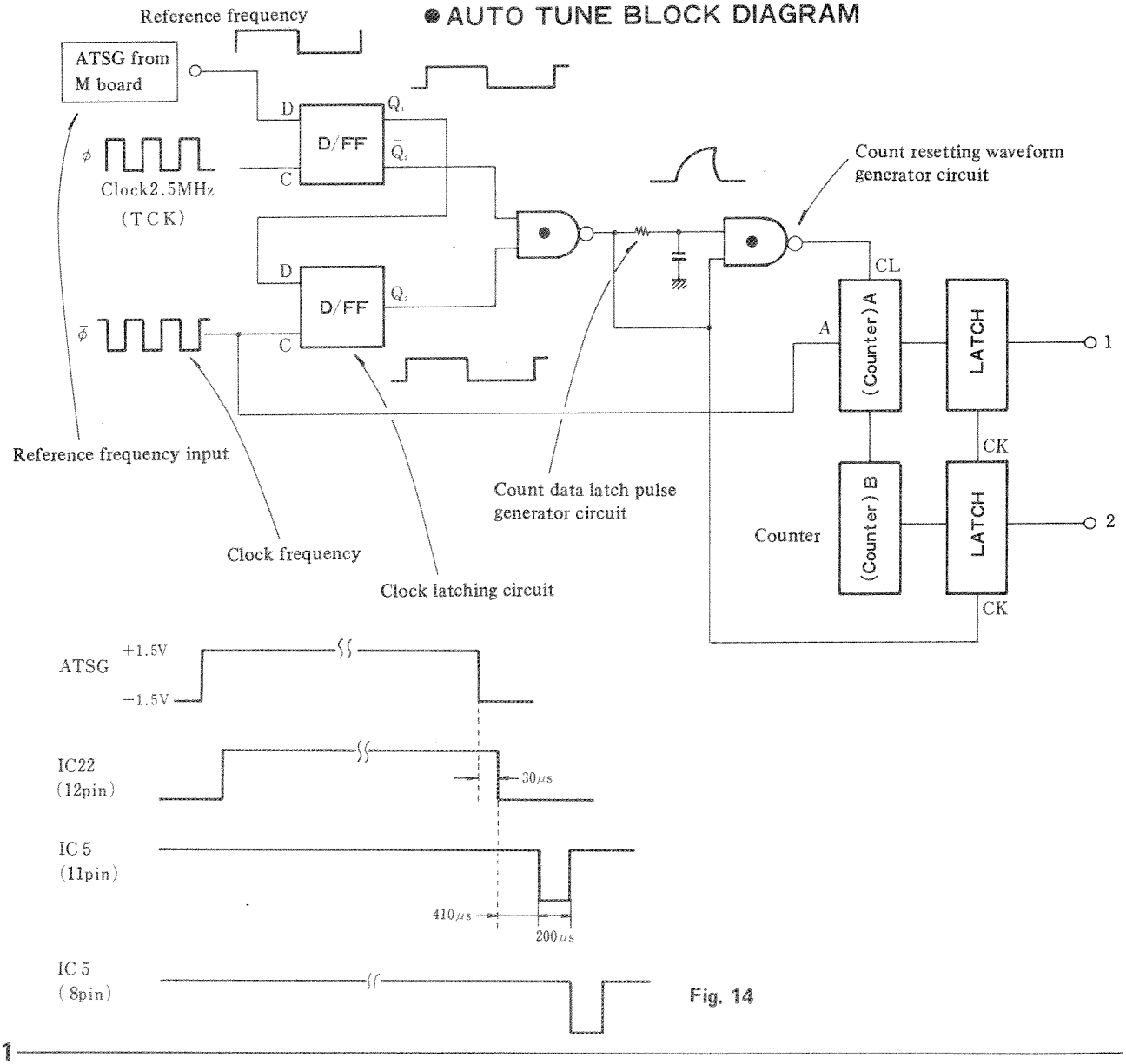


Fig. 14

Auto Tune Circuit Time Chart

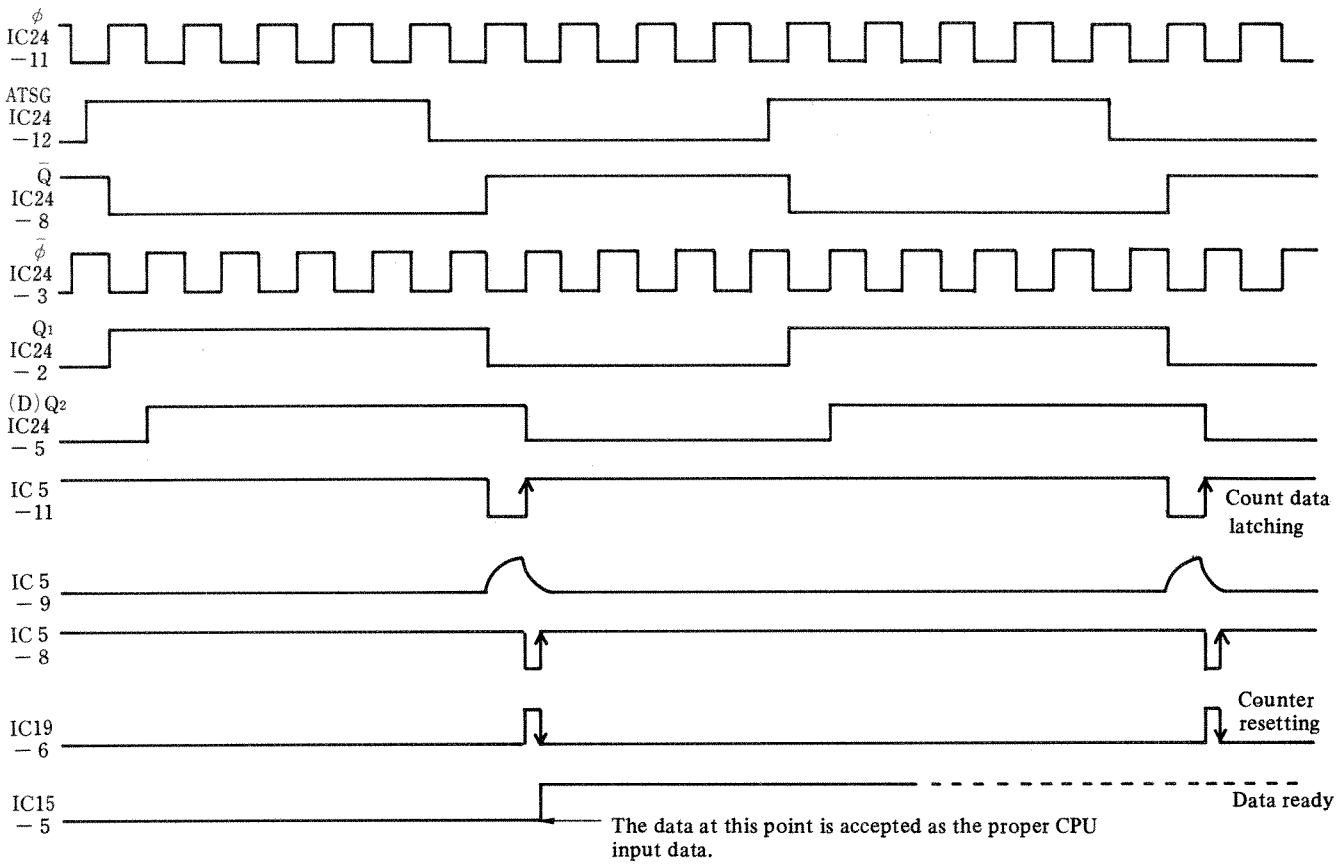


Fig. 15

Chart Description

A single cycle of M board output is counted by clocks. Data counted by IC25 and IC26 is latched by IC12 and IC13. The counter is then reset, and counting begins again. In other words, while data is being counted by IC25 and IC26, the previous data is being latched by IC12 and IC13. When the IC15-5 output is at high level, the count data is accepted as being correct by the CPU.

Furthermore, during auto tuning mode, low level from the DIF board is applied to (ATCN) and (ATN). Since this results in no application of LFO, the M board output is cut.

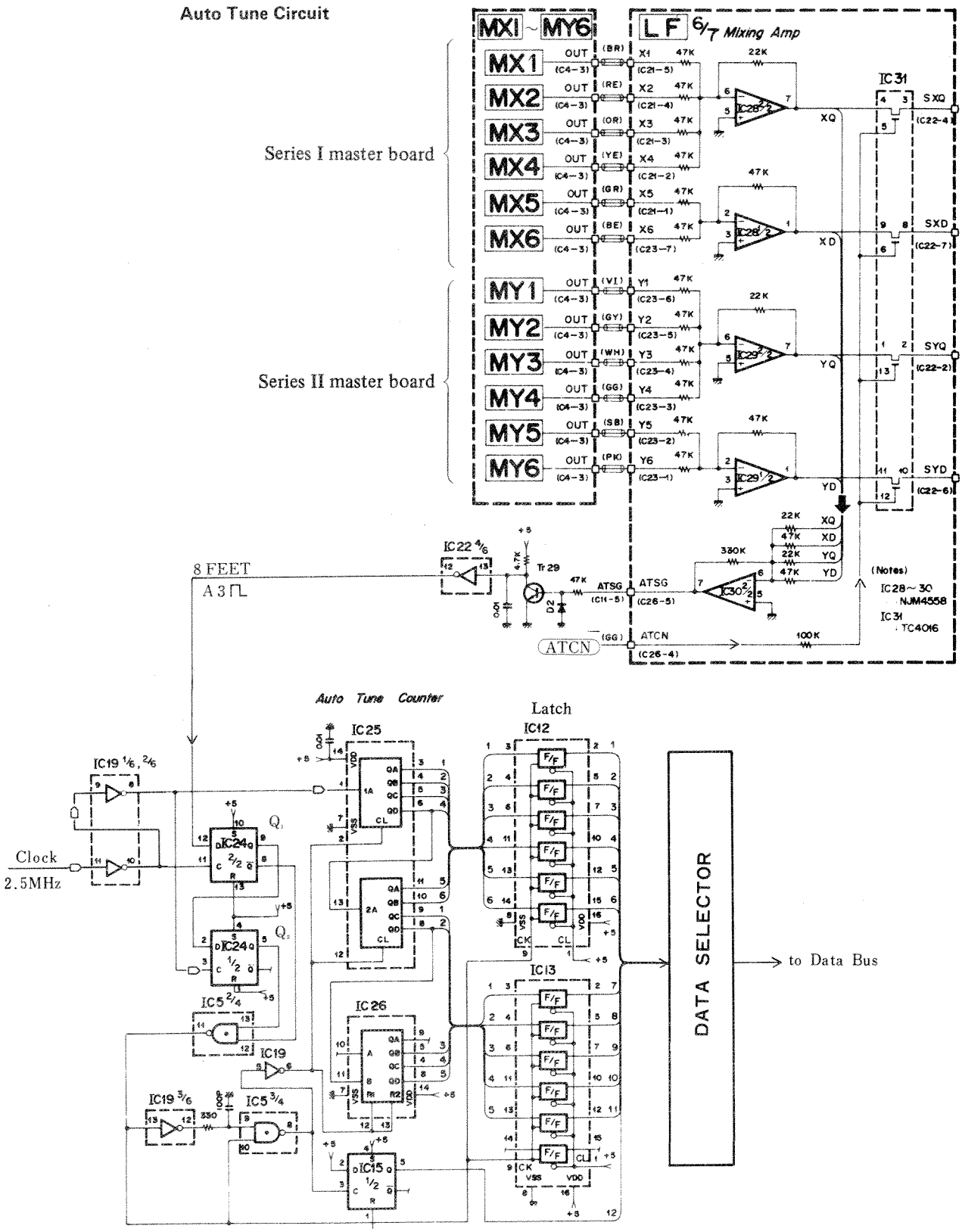

Auto Tune Circuit
MX1 ~ MY6
L F 6/7 Mixing Amp
Series I master board
Series II master board
MX1
MX2
MX3
MX4
MX5
MX6
MY1
MY2
MY3
MY4
MY5
MY6
IC31
SXQ
SXD
SYQ
SYD
XQ
XD
YQ
YD
(Notes)
IC28~30 NJM4558
IC31 TC4016
8 FEET
A3
ATSG
ATCN
100K
Auto Tune Counter
Latch
IC25
IC12
IC13
IC26
IC19
IC24
IC15
Clock
2.5MHz
DATA SELECTOR
to Data Bus

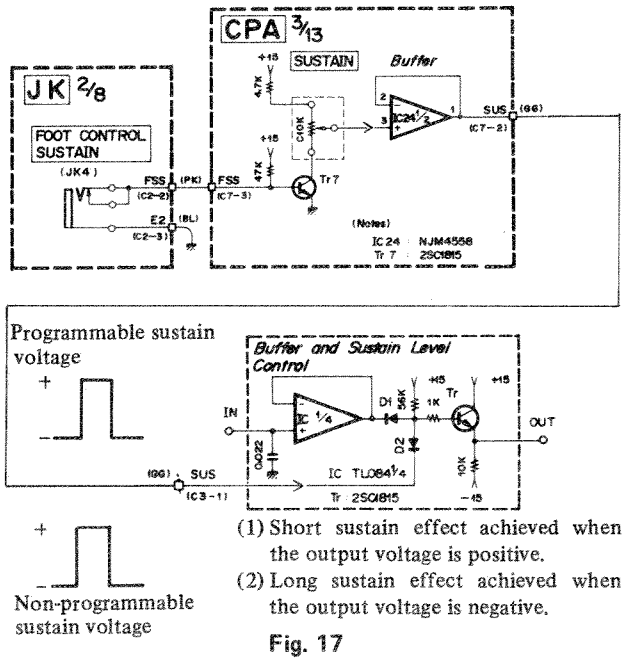
Fig. 16

Sustain Circuit (Service Manual pp. 8 ~ 10, 40, 58)

Sustained controlled can be achieved by either the VCA RELEASE TIME lever, or by the non-programmable sustain lever. A short sustain effect is achieved when a positive voltage appears at the sustain level control circuit output, while a long sustain effect is achieved when a negative voltage appears.

The following description refers to the case where the CPA SUSTAIN control lever is set to the E position. A voltage of +15V is applied via 4.7kΩ to the base of Tr7. This transistor is consequently turned on, resulting in voltage E appearing at buffer IC24 output pin no.1. This voltage is applied to the D2 cathode side of the sustain level control circuit, resulting in the transistor being turned off. The transistor output is thus dropped to −15V for a long sustain effect.

Sustain Circuit Diagram



(1) Short sustain effect achieved when the output voltage is positive.
(2) Long sustain effect achieved when the output voltage is negative.

Fig. 17

In the case of a short sustain effect, a reverse output voltage to the long sustain effect case is obtained at the transistor output.

As can be realized from the above description, the D2 control voltage has priority even when the programmable sustain control input is for a short sustain effect. So when the programmable sustain control is for a long sustain effect, the effect will be a long sustain.

External Key Code Interface Circuit

The major components of this circuit include a counter preset data circuit, a cable connection signal check circuit, a key code input flag, a key code input and counter circuit. The corresponding interfaces and address numbers are listed below.

External key Code Address Map

Address	I/O	Port
20	OUT	Counter preset data (IC23)
00	IN	Cable connection signal (IC43)
1A	IN	Key code input and flag (IC7, IC8, IC9)
1B	IN	Key code input (IC7, IC8, IC9)

When data is written into I/O address 20, i.e. IC23, the contents of bits 0 ~ 5 are latched by this IC23 and subsequently applied to the preset inputs of IC20 and IC21 (counter). This data is loaded in IC20 and IC21 by the trailing edge of CK0 (see Fig. 18), and then incremented by the trailing edges of CK1, CK2····· . When the 6-bit output of IC20 and IC21 is set to all "1" by the trailing edge of CKi (where i = 0, 1, ·····), CKi + 1 is inverted and subsequently obtained at the output of IC18 (NAND GATE), resulting in the key code being latched in IC10 and IC11 (LATCH) by the leading edge of CKi + 1. The CPU reads this key code via IC7, IC8 and IC9 (data selector) by reading I/O addresses 1A and 1B.

The flag consists of two flip-flop stages (IC14), bit 5 being obtained in I/O address 1A. The flag is reset by data writing in I/O address 20. The first stage flip-flop is set by the SY leading edge, and the second stage by the IC18 output pulse. The CN pin status is obtained in bit 7 of I/O address 00 IC43-2/2. The IC7, IC8, IC9 chips for address no.1 serve as a selector which selects one of the four data outputs in binary code. The functions of this selector are listed in Table 16 below.

IC Selector Function Table

B. A	G	Output(Y)
X X	H	Z
L L	L	C0
L H	L	C1
H L	L	C2
H H	L	C3

Table 16

The waveforms shown in the following diagram appear at the SY and CK pins.

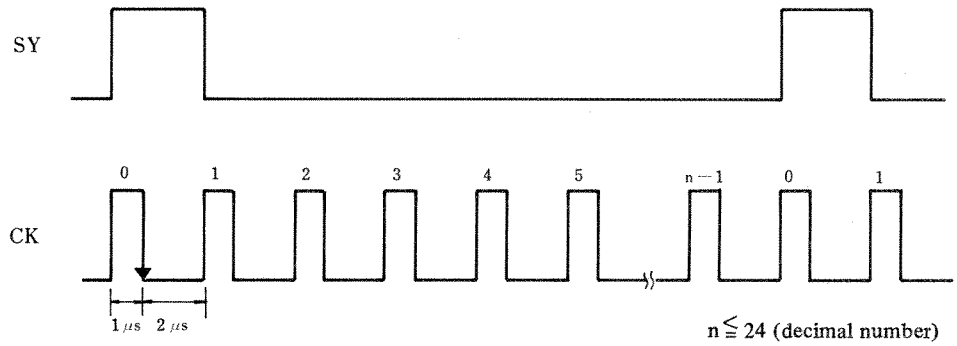


Fig. 18

Card Reader Circuit

The card reader includes a data control output circuit, a data switching input circuit and a flag circuit.

The data control output circuit is entirely LS-TTL open-collector. When data is written into I/O address 70, the contents of data bits 0 ~ 2 are inverted and obtained at MCS, MRS and RWC. And when bit 3 is 0, a symmetrical square wave signal with a 1.67μsec cycle appears at the WDT pin. When this bit is 1, however, the cycle time is halved. When the data switch input reads I/O address 12, the WPS and CLS pin status (H or L) is obtained by data bits 0 ~ 2. And if a suitable pulse is applied to DCP, the DDP status will be latched by this pulse, inverted, and be obtained by bit 3 of I/O address 12.

The output data accepted flag (1/2 IC33) is set by the leading edge of ACP, and reset by writing in CPU I/O address 70, the status appearing in bit 7 of I/O address 13. The input data ready flag (1/2 IC46) is set by the leading edge of the pulse applied to DCP and reset by reading CPU I/O address 12, the status appearing in bit 6 of I/O address 13.

The I/O address map for the card reader is outlined below.

Address	I/O	PORT
7 0	out	Data control (IC52)
1 2	in	Data switch (1.2 IC45)
1 3	in	Flag (1/2 IC45)

3. GENERAL OUTLINE OF THE Z80 CPU

The Z80 CPU is equipped with a 207-bit write/read memory designed to enable free accessing by the programmer. The memory array is shown in Table 17 below.

The registers include 16 (A ~ L) 8-bit registers and four 16-bit registers (index program counter). All Z80 registers consist of static RAMs. Two sets of 6 registers have been made available for independent use as 8-bit registers and also as 16-bit registers (in pairs). The internal block diagram is outlined in Fig. 19.

Table 17 Z80 Register Architecture

A (8 bit)	Flag F (8 bit)	A´	Flag F´
B (8 bit)	C (8 bit)	B´	C´
D (8 bit)	E (8 bit)	D´	E´
H (8 bit)	L (8 bit)	H´	L´

Interrupt Vector	Memory Reflesh
Index Resister IX	
Index Resister IY	
Stack Point Resister (SP)	
Program Counter (PC)	

Program Counter (PC)

The program counter maintains a 16-bit memory address for the instruction currently being executed. The CPU accepts an instruction from the memory address indicated by the PC. When the PC contents are passed out to the address bus, the PC value is automatically incremented by +1.

In the case of a program jump, a new value is set directly in the PC without any incrementing. In other words, it is the PC which stores in memory what address is to be executed next.

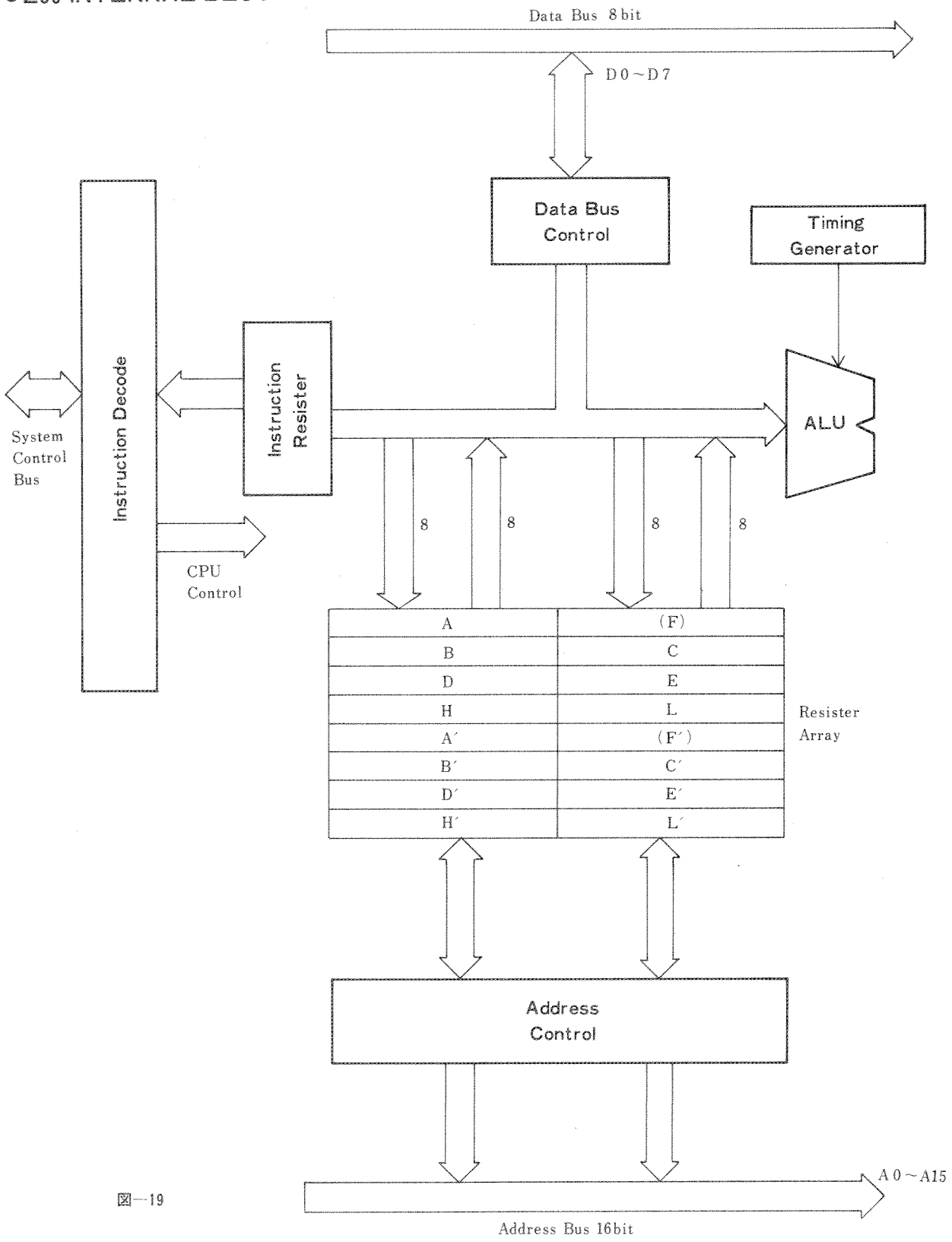
Stack Pointer (SP)

The purpose of the stack pointer is to maintain the most significant 16 bits at a certain point of time in the stack area in an external RAM. For example, when a subroutine is completed during the execution of a certain program, the point of return will not be known. For this reason, this stack is used, and the memory where the return address is stored is called the stack pointer.

Accumulators and Flag Registers

The CPU also contains two independent 8-bit accumulators and two corresponding 8-bit flag registers. These accumulators are memories which store the results of arithmetic and logical operations. The flag registers set the status of the 8-bit or 16-bit operation result (e.g. whether the result is equal to 0 or not).

● Z80 INTERNAL BLOCK



図—19

Z80 PIN DESCRIPTION

The Z-80A CPU is a standard 40-pin DIP package. The input/output pin layout diagram is shown below, and this is followed by a description of the individual pin functions.

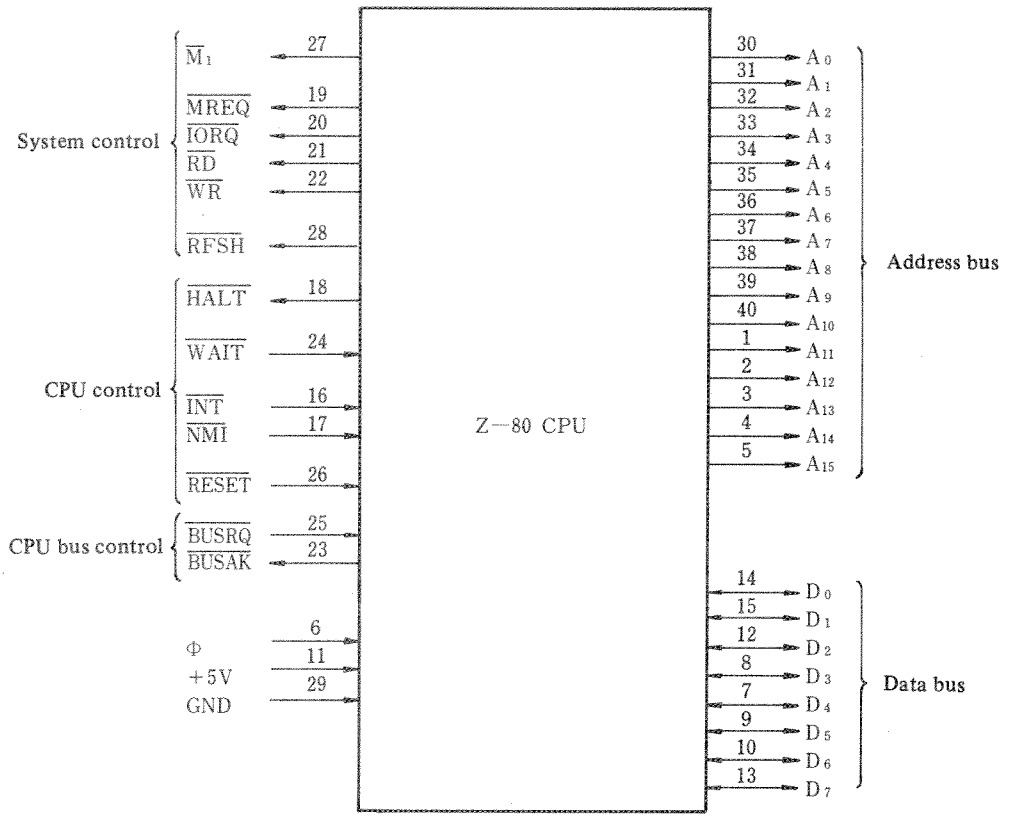


Fig. 20 Z-80A CPU Pin Layout

A0 ~ A15
(address bus)

Tri-state, active "H".
A0 ~ A15 constitute a 16-bit address bus employed in addressing for transfer of memory data (max. 64kbyte) and input/output device data. The least significant 8 bits are used for input/output addressing purposes. The user is able to directly select 256 input ports or 256 output ports. A0 is the LSB (least significant bit). During the refresh period, the actual refresh address is carried in the 7 least significant bits of the address bus.

D0 ~ D7
(data bus)

Tri-state input/output, active "H".
D0 ~ D7 constitute an 8-bit bidirectional data bus used for data exchange between memory, and input and output etc.

$\overline{M1}$
(machine cycle 1)

Output, active "L".
The $\overline{M1}$ output appears when the current machine cycle is the OP fetch cycle during instruction execution. It is to be kept in mind that the M1 output appears during each OP code fetch cycle during the execution of 2-byte OP codes. In instructions containing these 2-byte OP codes, the leading OP code starts with CBH, DDH, EDH or FDH.

The $\overline{M1}$ output also appears when an interrupt is acknowledged. $\overline{M1}$ and $\overline{IORQ}$ serve as the means whereby the CPU notifies external devices of interrupt acknowledgement.

$\overline{MREQ}$ (memory request)

Tri-state output, active "L".
The memory request output signal appears when the actual address for memory reading or memory writing is passed via the address bus.

$\overline{IORQ}$ (input/output request)

Tri-state, active "L".
The $\overline{IORQ}$ output signal appears when the actual input/output address for input/output reading or writing is carried by the 8 least significant bits of the address bus. Furthermore, like $\overline{M1}$, the $\overline{IORQ}$ output signal also appears when an interrupt is acknlwledged. These two signals are used to notify the input/output device that the interrupt response vector may be passed via the data bus. During the $\overline{M1}$ period, the interrupt acknowledge is processed without processing of the input/output device.

$\overline{RD}$ (memory read)

Tri-state output, active "L".
The $\overline{RD}$ output appears while the CPU is receiving data from memory or input/output device. The designated input/output device or memory data may be gated with this signal and passed via the CPU data bus.

$\overline{WR}$ (memory write)

Tri-state output, active "L".
The $\overline{WR}$ output appears when the data to be stored in the designated memory or input/output device is passed via the CPU data bus.

$\overline{RFSH}$ (refresh)

Output, active "L".
The $\overline{RFSH}$ output appears when the refresh address for dynamic memories is passed in the 7 least significant bits of the address bus. For refreshing of dynamic memories (refresh read), the $\overline{MREQ}$ signal is also required.

$\overline{HALT}$ (halt)

Output, active "L".
The $\overline{HALT}$ output appears when the CPU executes the $\overline{HALT}$ instruction and waits for a nonmaskable or maskable interrupt. A continuous output of refresh signals can be chieved during the halt period by CPU execution of the NOP instruction.

$\overline{WAIT}$ (wait)

Input, active "L".
This input signal is used to notify the CPU that the memory or input/output device is not ready to send data. The CPU maintains this wait status as long as the signal remains active. Note, however, that there is no output of refresh signals during this waiting period. Use of this signal enables synchronization of the CPU with the operating rate of any memory and any input/output device.

$\overline{INT}$
(interrupt request)

Input, active "L".
The interrupt request signal is generated input/output devices. The interrupt enable flag (IFF) can be set by software means (program), and if the $\overline{BUSRQ}$ signal is non-active, the interrupt request will be accepted as soon as the instruction currently being executed is completed. Upon reception of the interrupt, the CPU sends an acknowledge signal ($\overline{IORQ}$ during $\overline{M1}$ period) at the start of the next instruction cycle. A symmetrical square wave signal of 13.3msec cycle period is obtained at pin 11 of IC29.

$\overline{NM1}$
(nonmaskable interrupt)

Input, trailing edge detection.
The nonmaskable interrupt request has a higher priority than $\overline{INT}$. If this input is applied up to the leading edge of the final T cycle of the instruction currently being executed, the interrupt will be accepted following completion of that instruction. (This occurs irrespective of the status of the interrupt enable flag). The CPU is automatically restarted from the 0066_H address by the $\overline{NM1}$ input. The program counter contents are automatically saved in an external stack in order to ensure return to the original program where the interrupt was applied.
In the case of continuous WAIT cycles, $\overline{NM1}$ is made to wait, and note that $\overline{BUSRQ}$ has higher priority than $\overline{NM1}$.

$\overline{RESET}$

Input, active "L".
The program counter is reset to zero and the CPU initialized by the $\overline{RESET}$ input. At this time, the following status changes are made.
1) The interrupt enable flag is reset.
2) Register I is set to 00_H.
3) Register R is set to 00_H.
4) Interrupt mode 0 is set.
During this resetting period, the address bus and data bus are switched to high impedance, and all control outputs are switched to non-active status.

$\overline{BUSRQ}$
(bus request)

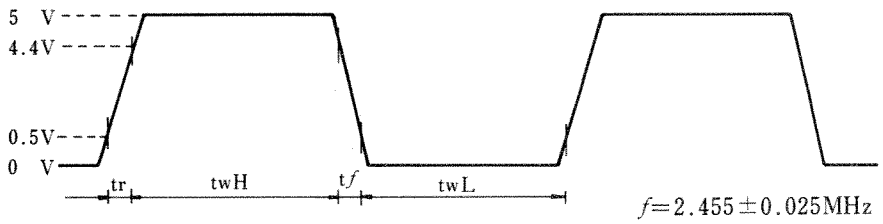
Input, active "L".
The bus request signal is used to switch the CPU address bus, data bus and tri-state output control lines to high impedance in order to enable other devices to utilize the buses. When $\overline{BUSRQ}$ is made active, the bus lines are switched to high impedance the moment the current CPU machine cycle is completed.

$\overline{BUSAK}$
(bus acknowledge)

Output, active "L".
The bus acknowledge output signal is passed to the bus-requesting external device after the CPU address bus, data bus and tri-state control bus lines have been switched to high impedance and may thus be utilized by the external device.

Φ

Single-phase TTL level clock input. The clock waveform is outlined in Fig. 21 below. This waveform signal appears at pin 6 of IC28.



$f=2.455\pm0.025$MHz

tr, $tf \leqq 25$ns twH, twL $\geqq 180$ns

Fig. 21

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● OVERALL BLOCK DIAGRAM

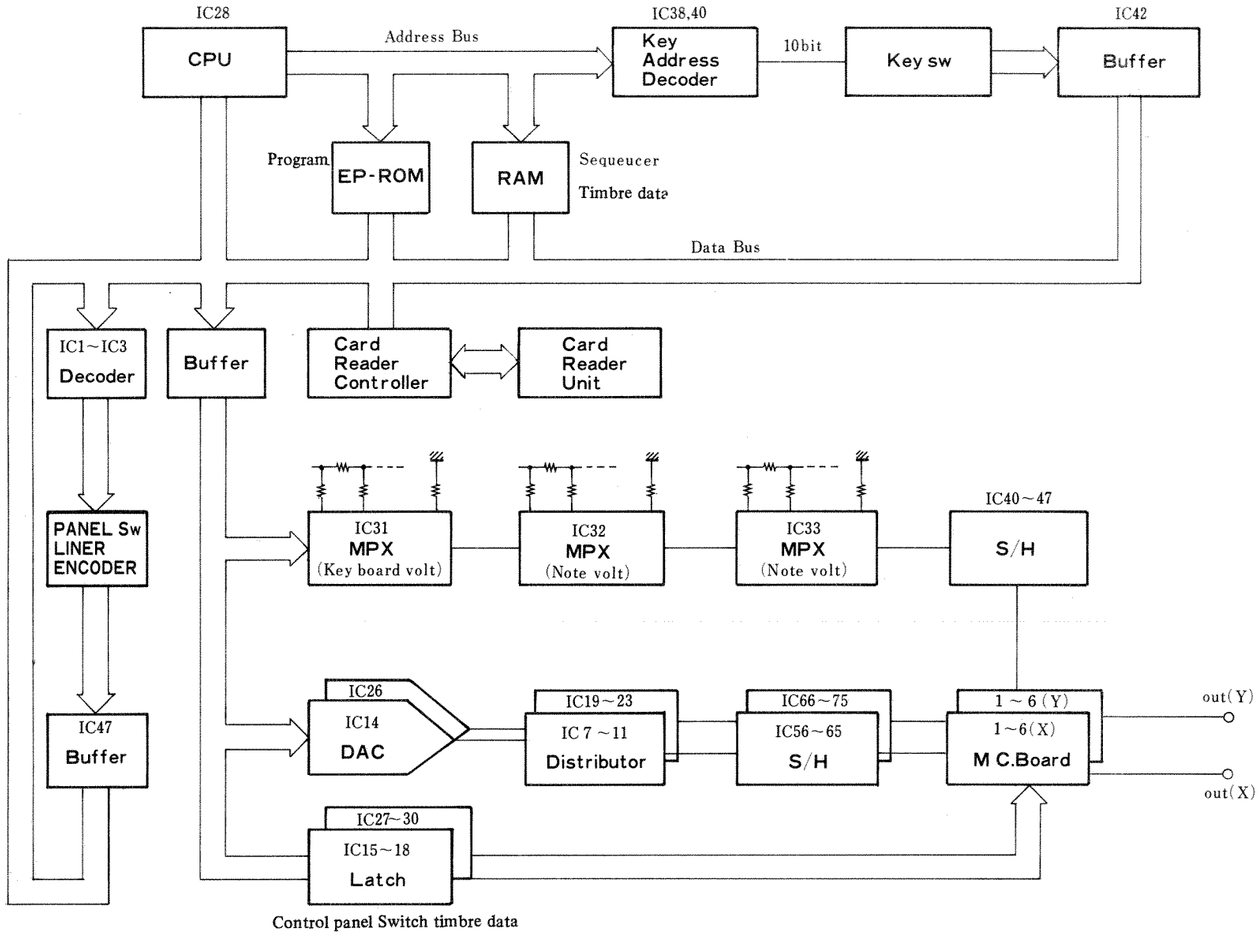


Fig. 2

● M Circuit Board Block Diagram

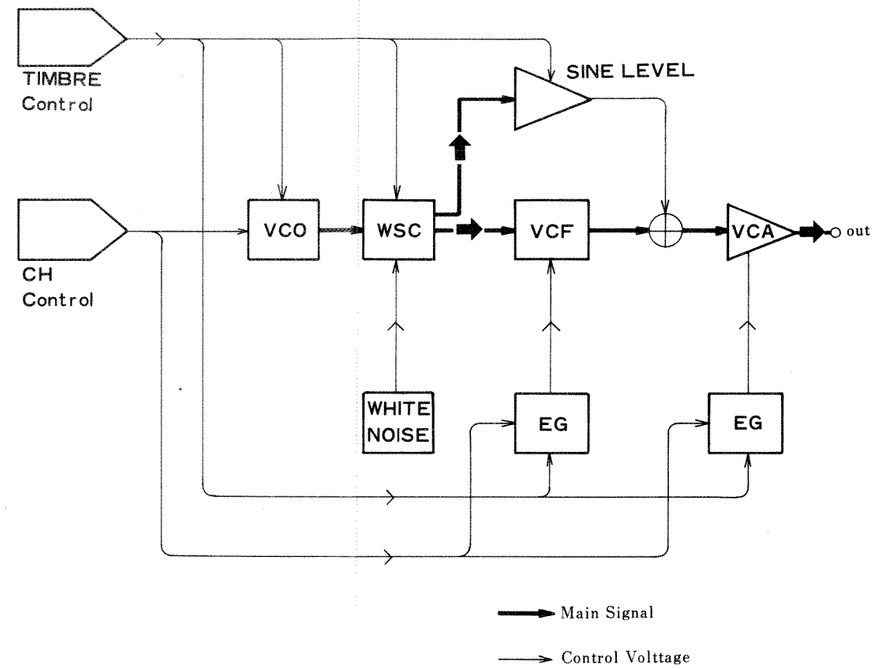


Fig. 3

2. INDIVIDUAL CIRCUIT DESCRIPTIONS

Refer to the Service Manual circuit diagrams and the overall diagram.

Keyboard Scanning Circuit (Service Manual pp. 32 ~ 34, 70, 71)

Unlike conventional synthesizers, the keyboard scanning circuit in the CS70M involves an initial passing of 3-bit address signals from the CPU to the IC38/IC40 keyboard address decoder for addressing. The decoder used here is an IC chip where low level outputs are obtained only when the enable input G1 = H and G2A = G2B (see Table 3). Furthermore, this output is switched to low voltage in succession, generating 10 scanning bits by using another IC chip.

This 10-bit output voltage is then inverted by the data bus buffer, and applied to the respective half-octave terminals of the manual keyboard. If any of the keys is then turned on under these conditions, the key switch is short circuited, and the scanning result subsequently appears at the N1 ~ N7 terminals via a diode circuit.

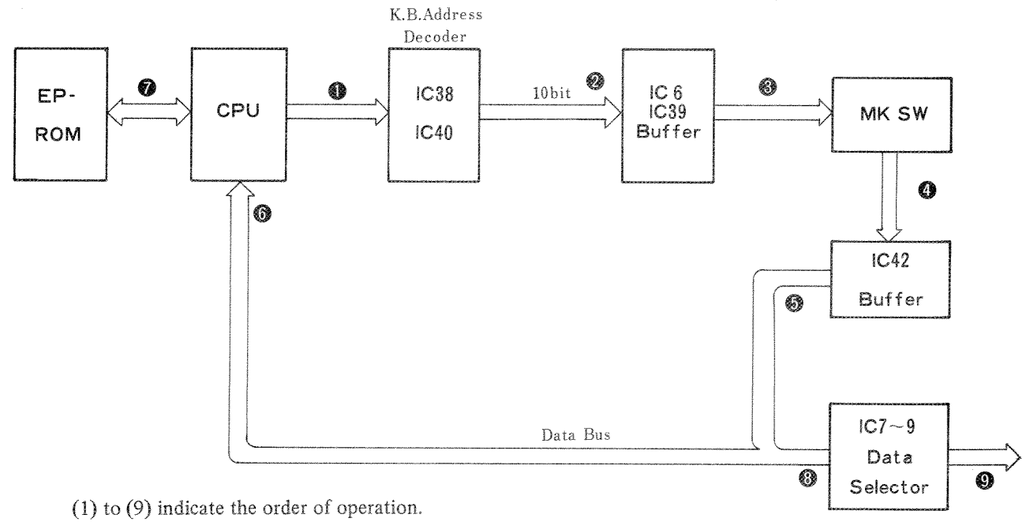
Decoder Table (for IC single-chip)

Enable		Address Input	Output							
G_1	G_{2A}	C B A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
H	L	L L L	L	H	H	H	H	H	H	H
H	L	L L H	H	L	H	H	H	H	H	H
H	L	L H L	H	H	L	H	H	H	H	H
H	L	L H H	H	H	H	L	H	H	H	H
H	L	H L L	H	H	H	H	L	H	H	H
H	L	H L H	H	H	H	H	H	L	H	H
H	L	H H L	H	H	H	H	H	H	L	H
H	L	H H H	H	H	H	H	H	H	H	L

Table 3

Octaves and notes are thus scanned by the KBD0 ~ KBD9 and N1 ~ N7 terminal matrix, and the results passed to the CPU via the CPU data bus. The CPU addresses key code data in the EP-ROM on the basis of the data bus results, the key code finally being passed to the data selector via the data bus. These steps are summarized in the block diagram in Fig. 4.

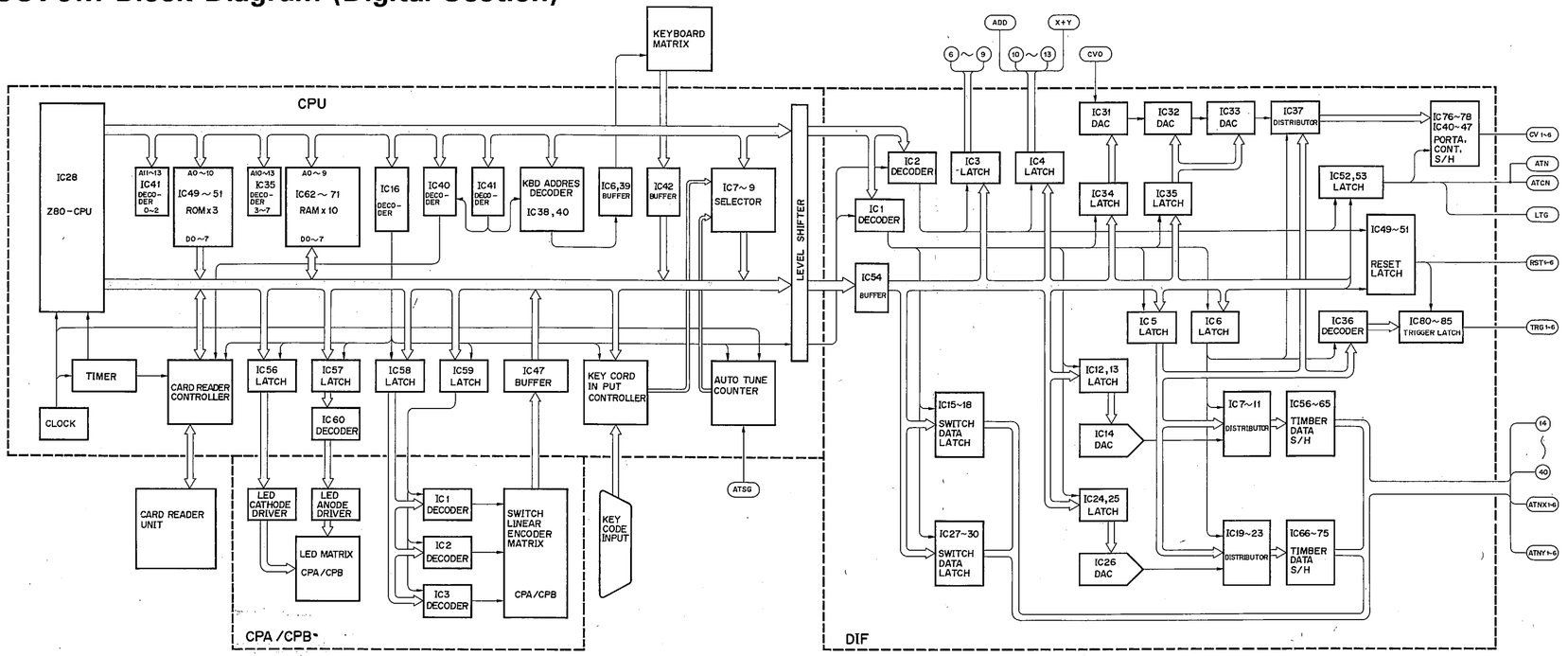
● Key board Scan. Block Diagram



(1) to (9) indicate the order of operation.

Fig. 4

CS70M Block Diagram (Digital Section)



Block Diagram (Analog Section)